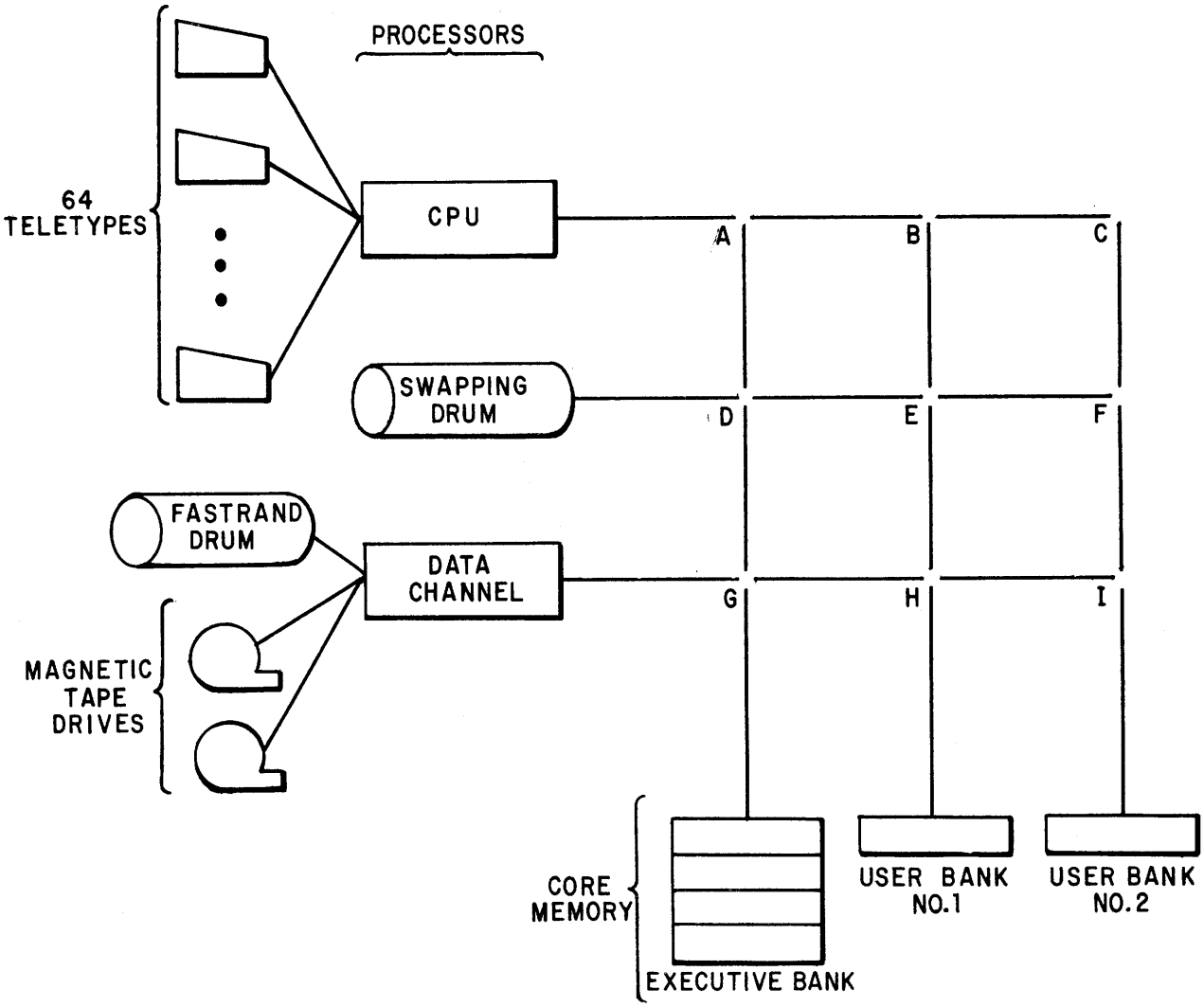

FIGURE 1. Interconnection of processors and memory banks.

Each of the points on the Figure, labeled A through I, is a possible processor/memory connection. For example, at some time connections might be made at points B and F; in this case, the program in User Memory Bank No. 1 is running while another program is being swapped into User Memory Bank No. 2. At another time, connections might be made at points A, E, and I; this is the case where the routines in Executive Memory are handling interrupts, the program in User Memory Bank No. 2 is performing a bulk-storage I-O operation via the Data Channel, and another program is being swapped into User Memory Bank No. 1.